ABSTRACT

A dynamic test generation method and apparatus enabling verification of the parallel instruction execution capabilities of VLIW processor systems is described. The test generator includes a user preference queue, a rules table, plurality of resource-related data structures, an instruction packer, and an instruction generator and simulator. The present invention generates a test by selecting instructions for parallel execution based upon resource availability as indicated by the resource-related data structures and the processor's instruction grouping rules, simulating the parallel execution of the instructions on a golden model, updating the resource-related data structures, and evaluating the updated architectural state of the golden model.